REMARKS

Claims 1-20 are pending in this application.

The Office Action rejects claims 1-20 under 35 U.S.C. §102(d) over U.S. Patent 5,301,325 to Benson. This rejection is respectfully traversed.

The Office Action asserts that Benson discloses a controller dividing the source code into translated code blocks of the target code based on a target processor register capability, as recited in claims 1 and 11. However, Applicants submit that Benson does not disclose such a controller.

The Office Action cites col. 4, lines 13-18 and col. 4, lines 67-68 - col. 5, lines 1-18 of Benson, which discloses that "The input code is parsed to determine its content, with the basic building blocks of the code identified (separated) and converted into an intermediate language. The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine...In code generated by the compiler for register saves for an advanced 64-bit RISC architecture, only the low 32-bits of the 64-bit register can be put on the stack...Accordingly, in one embodiment of the invention, the compiler tracks register usage to determine which registers are destroyed by a routine, and generate routine prologue and epilogue code which performs 64-bit register saves."

Benson is silent as to whether the structure or organization of these routines is based on target processor register capability, or whether the flow analyzer techniques are based on target processor register capability. Instead Benson merely discloses that the compiler generates prologue and epilogue code which performs a 64-bit register save on registers which are determined to be destroyed by a routine. Benson does not disclose that the code

generated by the compiler is divided into code blocks based on the target processor register capability, as recited in claim 1.

Therefore, the subject matter recited in claim 1 is not anticipated by Benson. Therefore, Applicants respectfully request that the rejection of independent claim 1 and dependent claims 2-10 be withdrawn.

The Office Action rejects claims 11-20 under 35 U.S.C. §102(b) over Benson. However, claim 11 recites the same patentable feature as was recited in claim 1, wherein "dividing the source code into translated code blocks of the target code based on the target processor register capability." Therefore, claim 11 recites patentable subject matter for similar reasons set forth above. Applicants respectfully request that the rejection of independent claim 11 and dependent claims 12-20 be withdrawn.

In view of the foregoing, Applicants submit that this application is in condition allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the Applicants' attorney at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jaquelin K. Spong
Registration No. 52,241

JAO:JKS/gew

Application No. 09/558,542

Date: May 15, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461